

TITLE 400G QSFP-DD SR4 Transceiver	DOC No. RFD-20240808013-001	
	REVISION : 01	AUTHORIZED BY : Andy Yang
	DATE : 2024.08.09	CLASSIFICATION : Optics Transceiver

1. PRODUCT FEATURES

- Hot-pluggable QSFP-DD multimode transceiver
- Optical Interface Compliant with IEEE802.3db
- Electric Interface Compliant with IEEE802.3ck
- 4-channels of 100G-PAM4 optical modulation
- Reach up to 30m on MMF(OM3) or 50m on MMF(OM4)
- 850nm VCSEL laser and PIN receiver
- Compliant with QSFP-DD CMIS Rev 4.0
- Compliant with QSFP-DD MSA HW Rev 5.1
- Maximum power consumption 7W
- Single 3.3V power supply
- Case operating temperature 0°C to 70°C
- Compliant to RoHS
- Class 1 laser Safety



2. PRODUCT DESCRIPTION

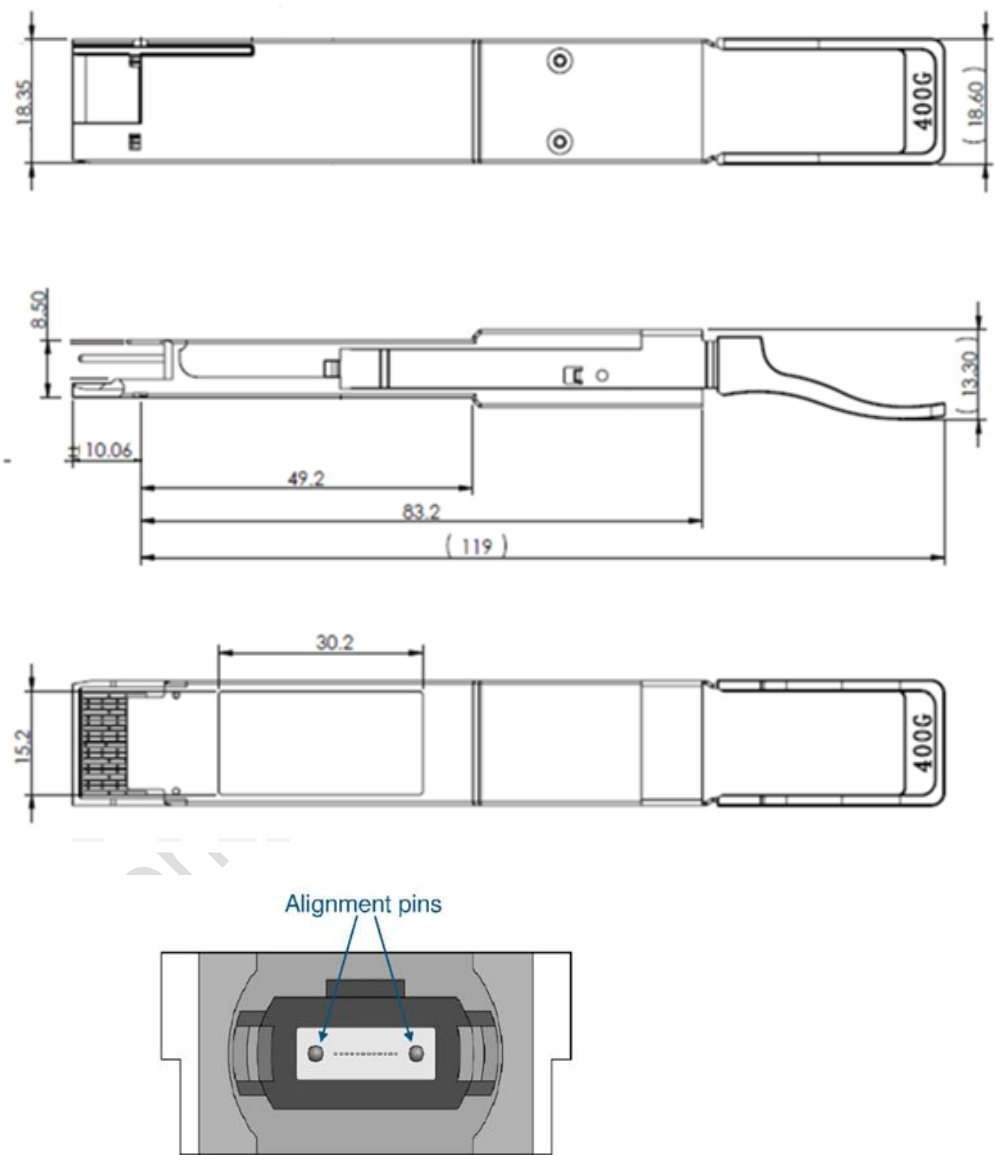
2.1 PRODUCT NAME

400G QSFP-DD SR4 Transceiver

Data Rate	Wavelength (nm)	Distance	Optical Power	Sensitivity	Connector	Temp.
400G	850	30m (OM3) 50m (OM4)	-4.6 ~ 4 dBm	-4.4 dBm	MPO-12	C

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2.2 DIMENSIONS, MATERIALS, PLATINGS AND MARKING



Transmit Channels: 1 2 3 4
Unused positions: x x x x
Receive Channels: 4 3 2 1

Unit is millimeter. All dimensions are mm unless otherwise specified.

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3. APPLICABLE DOCUMENTS AND SPECIFICATIONS

- 400G Ethernet
- Data Center Interconnect
- Enterprise Networking

4. Product specifications

4.1 Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit	Notes
Storage Temperature	T _S	-40	85	°C	
Power Supply Voltage	V _{CC}	-0.5	3.6	V	
Control Input Voltage	V _I	-0.3	V _{CC} +0.5	V	
Relative Humidity (non-condensing)	RH	5	95	%	

4.2 Recommended Operating Conditions

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Operating Case Temperature	T _{OPR}	0	-	70	°C	
Power Supply Voltage	V _{CC}	3.135	3.3	3.465	V	
Instantaneous peak current at hot plug	ICC_IP	-	-	3600	mA	
Sustained peak current at hot plug	ICC_SP	-	-	3000	mA	
Maximum Power Dissipation(400G)	PD	-	-	7	W	
Maximum Power Dissipation, Low Power Mode	PDLP	-	-	1.5	W	
Signaling Rate per Lane	SRL	-	53.125	-	GBd	PAM4
Two Wire Serial Interface Clock Rate	-	-	-	400	kHz	
Power Supply Noise Tolerance (10Hz - 10MHz)	-	-	-	66	mV	
Rx Differential Data Output Load	-	-	100	-	Ohm	
Operating Distance (OM3)	-	2	-	30	m	
Operating Distance (OM4)	-	2	-	50	m	

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4.3 Transmitter Optical Specifications

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Center Wavelength	λ_C	844	850	863	nm	
RMS spectral width	$\Delta\lambda_{rms}$			0.6	nm	
Average launch power, each lane	AOPL	-4.6		4.0	dBm	1
Outer Optical Modulation Amplitude (OMA _{outer}), each lane	TOMA	-2.6		3.5	dBm	2
Transmitter and dispersion eye closure for PAM4 (TDECQ), each lane	TDECQ			4.4	dB	
Average Launch Power of OFF Transmitter, each lane	T _{OFF}			-30	dBm	
Extinction ratio, each lane	ER	2.5	-	-	dB	
RIN _{21.4OMA}	RIN	-	-	-132	dB/Hz	
Transmitter Reflectance	TR	-	-	-26	dB	3
Optical return loss tolerance		-	-	-12	dB	

Notes

1. Average launch power, each lane (min) is informative and not the principal indicator of signal strength.
2. Even if max (TECQ, TDECQ) < 1.8dB, OMA_{outer} (min) must exceed this value.
3. Transmitter reflectance is defined looking into the transmitter.

4.4 Receiver Optical Specifications

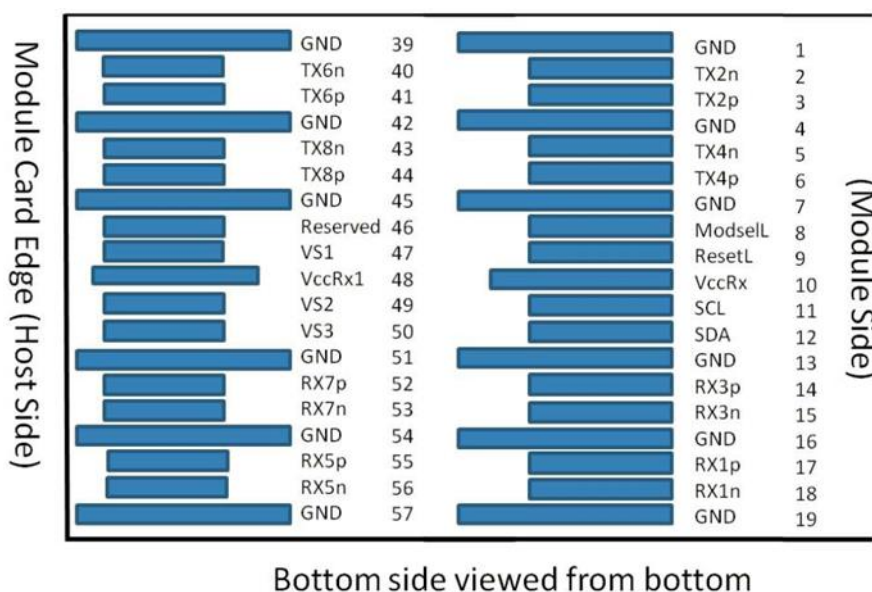
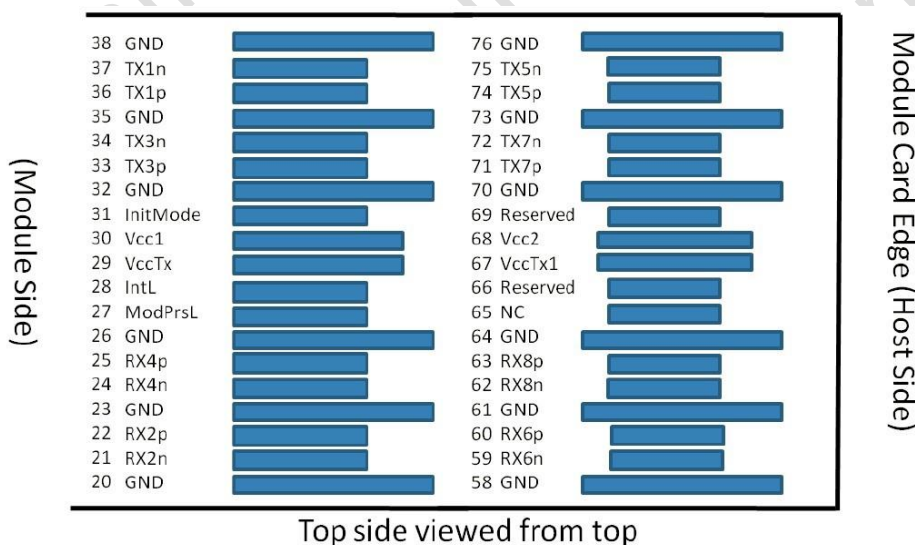
Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Center Wavelength	λ_C	842	-	863	nm	
Average receive power, each lane	AOP _R	-6.3	-	4	dBm	1
Receive power, each lane (OMA _{outer})	OMA _R	-	-	3.5	dBm	
Receiver reflectance	R _R		-	-26	dB	
Receiver sensitivity (OMA _{outer}), each lane	S _{OMA}		-	-4.4	dBm	2
Stressed receiver sensitivity (OMA _{outer}), each lane	SRS		-	-1.8	dBm	3
Conditions of stressed receiver sensitivity test						
Stressed eye closure for PAM4	SECQ		4.4		dB	
OMA _{outer} of each aggressor lane	OMA _{outer}		3.5		dBm	

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Notes:

- 1.Minimum power is informative. AOP above the minimum does not ensure compliance
- 2.Receiver sensitivity (OMAouter), each lane (max) is informative and is defined for a transmitter with SECQ of 0.9 dB.
- 3.Measured with conformance test signal at TP3 for the BER = 2.4x10-4

5. QSFP-DD Edge Connector and Pinout Description



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Pin Definition

Pin #	Logic	Symbol	Description	Pin #	Logic	Symbol	Description
1		GND	Ground	39		GND	Ground
2	CML-I	Tx2n	Transmitter Inverted Data Input	40	CML-I	Tx6n	Transmitter Inverted Data Input
3	CML-I	Tx2p	Transmitter Non-inverted Data Input	41	CML-I	Tx6p	Transmitter Non-inverted Data Input
4		GND	Ground	42		GND	Ground
5	CML-I	Tx4n	Transmitter Inverted Data Input	43	CML-I	Tx8n	Transmitter Inverted Data Input
6	CML-I	Tx4p	Transmitter Non-inverted Data Input	44	CML-I	Tx8p	Transmitter Non-inverted Data Input
7		GND	Ground	45		GND	Ground
8	LVTTL-I	ModSelL	Module Select	46		Reserved	
9	LVTTL-I	ResetL	Module Reset	47		VS1	Module Vendor Specific 1
10		VccRx	+3.3V Power Supply Receiver	48		VccRx1	3.3V Power Supply
11	LVC MOS -I/O	SCL	2-wire serial interface clock	49		VS2	Module Vendor Specific 2
12	LVC MOS -I/O	SDA	2-wire serial interface data	50		VS3	Module Vendor Specific 3
13		GND	Ground	51		GND	Ground
14	CML-O	Rx3p	Receiver Non-inverted Data Output	52	CML-O	Rx7p	Receiver Non-inverted Data Output
15	CML-O	Rx3n	Receiver Inverted Data Output	53	CML-O	Rx7n	Receiver Inverted Data Output
16		GND	Ground	54		GND	Ground
17	CML-O	Rx1p	Receiver Non-inverted Data Output	55	CML-O	Rx5p	Receiver Non-inverted Data Output
18	CML-O	Rx1n	Receiver Inverted Data Output	56	CML-O	Rx5n	Receiver Inverted Data Output
19		GND	Ground	57		GND	Ground
20		GND	Ground	58		GND	Ground
21	CML-O	Rx2n	Receiver Inverted Data Output	59	CML-O	Rx6n	Receiver Inverted Data Output
22	CML-O	Rx2p	Receiver Non-inverted Data Output	60	CML-O	Rx6p	Receiver Non-inverted Data Output
23		GND	Ground	61		GND	Ground
24	CML-O	Rx4n	Receiver Inverted Data Output	62	CML-O	Rx8n	Receiver Inverted Data Output
25	CML-O	Rx4p	Receiver Non-inverted Data Output	63	CML-O	Rx8p	Receiver Non-inverted Data Output
26		GND	Ground	64		GND	Ground
27	LVTTL-O	ModPrsL	Module Present	65		NC	Not connected
28	LVTTL-O	IntL	Interrupt	66		Reserved	

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29		VccTx	+3.3V Power Supply Transmitter	67		VccTx1	3.3V Power Supply
30		Vcc1	+3.3V Power Supply	68		Vcc2	3.3V Power Supply
31	LVTTTL-I	InitMode	Initialization mode	69		Reserved	
32		GND	Ground	70		GND	Ground
33	CML-I	Tx3p	Transmitter Non-inverted Data Input	71	CML-I	Tx7p	Transmitter Non-inverted Data Input
34	CML-I	Tx3n	Transmitter Inverted Data Input	72	CML-I	Tx7n	Transmitter Inverted Data Input
35		GND	Ground	73		GND	Ground
36	CML-I	Tx1p	Transmitter Non-inverted Data Input	74	CML-I	Tx5p	Transmitter Non-inverted Data Input
37	CML-I	Tx1n	Transmitter Inverted Data Input	75	CML-I	Tx5n	Transmitter Inverted Data Input
38		GND	Ground	76		GND	Ground

6. Modification History

Rev.	Comments	Date	Originator	Approval
01	Preliminary Draft	2024.08.09	Andy Yang	Mike Sun